1. A process for filling an opening, comprising:

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

depositing a first seed layer of metal to a first thickness to coat the integrated circuit upper surface, the bottom surface, and the side walls of the opening;

sputter etching said first seed layer, to reduce its thickness by a first amount, thereby preferentially removing some overhanging material present at the mouth of the opening;

depositing a second seed layer over said first seed layer ;

sputter etching said second seed layer to reduce its thickness by a second amount, thereby preferentially removing any remaining overhanging material present at the mouth of the opening; and

depositing additional metal, whereby said opening becomes completely filled with void free metal.

2. The process described in claim 1 wherein said first thickness is between about 800 and 2,500 Angstroms.

3. The process described in claim 1 wherein said first amount by which thickness is reduced is between about 400 and 1,000 Angstroms.

4. The process described in claim 1 wherein said second amount by which thickness is reduced is between about 400 and 1,000 Angstroms.

5. A damascene process resulting in improved side wall coverage, comprising:

providing a dielectric layer, having an upper surface, on an integrated circuit;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls;

depositing a first seed layer of copper to a first thickness to coat said upper surface, said bottom surface, and said side walls;

sputter etching said first seed layer, to reduce its thickness by a first amount, thereby preferentially removing some overhanging material present at the mouth of the trench;

depositing a second seed layer on said first seed layer ;

sputter etching said second seed layer to reduce its thickness by a second amount, thereby preferentially removing any remaining overhanging material present at the mouth of the trench;

depositing additional copper to form a filler layer that overfills the trench; and

planarizing said filler layer, thereby just filling the trench with copper and removing any copper that is outside the trench.

6. The process described in claim 5 wherein said first thickness is between about 800

and 2,500 Angstroms.

7. The process described in claim 5 wherein said first amount by which thickness is reduced is between about 400 and 1,000 Angstroms.

8. The process described in claim 5 wherein said second amount by which thickness is reduced is between about 400 and 1,000 Angstroms.

9. A dual damascene process comprising:

on a first wiring layer, providing a dielectric layer having an upper surface and a thickness;

forming a via hole that extends from said upper surface to said first wiring layer;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls, said trench being disposed so as to fully overlap said via hole and to extend a depth below said upper surface, said depth being between about 0.5 and 2 times said dielectric thickness whereby said via hole extends a distance from said trench bottom surface that is between about 0.5 and 2 times said dielectric thickness;

by means of PVD, depositing a seed layer of metal to coat the dielectric layer, said bottom surface, and said side walls;

sputter etching the seed layer, to reduce its thickness by an amount, thereby

preferentially removing any overhang present at the mouth of the trench;

depositing metal to form a filler layer that overfills the trench and via hole; and

planarizing said filler layer, thereby just filling the trench with metal, forming a second wiring layer, removing any metal that is outside the trench, and forming a metal via whose aspect ratio is less than about 6:1 whereby its electrical resistance is less than about 0.1 ohms.

10. The process described in claim 9 wherein the metal is selected from the group consisting of copper, gold, and silver.

11. The process described in claim 9 wherein the metal is copper and said electrical resistance is less than about 1 ohm.

12. A process for filling an opening, comprising:

providing a power supply having high and low voltage settings;

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

in said sputtering chamber, by connecting a metal target to said power supply, set to high voltage, sputter depositing a seed layer of metal to coat the integrated circuit upper

surface, the bottom surface, and the side walls of the opening;

then, in said sputtering chamber, by connecting said integrated circuit to said power supply set to low power and voltage, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening; and

depositing additional metal, whereby said opening becomes completely filled with void free metal.

13. The process described in claim 12 wherein said power is between about 1 and 1KW and 50KW.

14. A damascene process resulting in improved side wall coverage, comprising:

providing a power supply having high and low voltage settings;

providing a dielectric layer, having an upper surface, on an integrated circuit;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

in said sputtering chamber, by connecting a copper target to said power supply, set to high voltage and power, sputter depositing a seed layer of copper to coat said upper surface, said bottom surface, and the side walls of the trench;

then, in said sputtering chamber, by connecting said integrated circuit to said power

supply set to low voltage, sputter etching the seed layer to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the trench;

depositing additional copper to form a filler layer that overfills the trench; and

planarizing said filler layer, thereby just filling the trench with copper and removing any copper that is outside the trench.

15. The process described in claim 14 wherein said power is between about 1KW and 50KW.

16 . A process for filling an opening, comprising:

providing a power supply having high and low voltage settings;

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

at a first sputtering gas pressure between about 0.1 and 10 mtorr in said sputtering chamber, by connecting a metal target to said power supply set to high voltage and power, sputter depositing a seed layer of metal to coat the integrated circuit upper surface, the bottom surface, and the side walls of the opening;

then, at a second sputtering gas pressure between about 10 and 90 mtorr, in said sputtering chamber, by connecting said integrated circuit to said power supply set to low

voltage, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening; and

depositing additional metal, whereby said opening becomes completely filled with void free metal.

17. The process described in claim 16 wherein said sputtering gas is argon.

18. The process described in claim 16 wherein said amount that thickness is reduced is between about 400 and 1,000 Angstroms.

19. A damascene process resulting in improved side wall coverage, comprising:

providing a power supply having high and low voltage settings;

providing a dielectric layer, having an upper surface, on an integrated circuit;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

at a first sputtering gas pressure between about 0.1 and 10 mtorr in said sputtering chamber, by connecting a copper target to said power supply set to high voltage and power, sputter depositing a seed layer of copper to coat said upper surface, the bottom surface, and the side walls of the trench;

then, at a second sputtering gas pressure between about 10 and 90 mtorr, in said

sputtering chamber, by connecting said integrated circuit to said power supply set to low voltage and power, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening; and

depositing additional copper to form a filler layer that overfills the trench; and

planarizing said filler layer, thereby just filling the trench with copper and removing any copper that is outside the trench.

20. The process described in claim 19 wherein said sputtering gas is argon.

21. The process described in claim 19 wherein said amount that thickness is reduced is between about 400 and 1,000 Angstroms.

22. A process for filling an opening, comprising:

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

by means of PVD, depositing a seed layer of metal to coat the integrated circuit upper surface, the bottom surface, and the side walls of the opening;

at a first pressure between about 0.1 and 10 mtorr, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening;

at a second pressure between about 10 and 90 mtorr, re-depositing said seed layer by means of sputter deposition, thereby replacing said amount removed without re-introducing said overhang; and

depositing additional metal, whereby said opening becomes completely filled with void free metal.

23. The process described in claim 22 wherein argon is used to implement said steps of sputter etching and sputter deposition.

24. The process described in claim 22 wherein said amount that thickness is reduced is between about 400 and 1,000 Angstroms.

25. A damascene process resulting in improved side wall coverage, comprising:

providing a dielectric layer on an integrated circuit;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls;

by means of PVD, depositing a seed layer of copper to coat the dielectric layer, said bottom surface, and said side walls;

at a first pressure between about 0.1 and 10 mtorr, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening;

at a second pressure between about 10 and 90 mtorr, re-depositing said seed layer by means of sputter deposition, thereby replacing said amount removed without re-introducing said overhang;

depositing additional copper to form a filler layer that overfills the trench; and

planarizing said filler layer, thereby just filling the trench with copper and removing any copper that is outside the trench.

26. The process described in claim 25 wherein argon is used to implement said steps of sputter etching and sputter deposition.

27. The process described in claim 25 wherein said amount that thickness is reduced is between about 400 and 1,000 Angstroms.